Applicants' attorney would like to thank Examiner Sarkar for his time and courtesy during the interview conducted on March 13, 2003. It is noted that Examiner Sarkar indicated that he would generate an Interview Summary Record.

II. The Rejection Of Claims 1, 3, 5, 6, 20, 22, 24 And 25 Under 35 U.S.C. § 103

Claims 1, 3, 5, 6, 20, 22, 24 and 25 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era. Applicants respectfully traverse this rejection for the following reasons.

With regard to claims 1 and 20, which are the only independent claims contained in the foregoing rejection, both of these method claims recite the step ***of applying a first voltage to an impurity solid***. In the pending rejections, Booske is relied upon as disclosing this element of the method claims. However, it is respectfully submitted that this conclusion is incorrect. Booske does not appear to disclose applying any type of voltage to the impurity solid. As set forth on col. 9, lines 14-21, Booske discloses firing ions at the target 46 (i.e., impurity solid) by means of an ion source 44 in order to sputter the target material and form the thin layer 38. As agreed upon during the interview, it is not necessary for the impurity solid 46 of Booske to have a voltage applied thereto to accomplish the firing of ions at the target 46.

Thus, at a minimum, Booske fails to disclose or suggest this limitation recited by both claims 1 and 20. It is noted that Wolf is not relied upon as curing the foregoing deficiency of Booske in the pending rejection.

Furthermore, claims 1 and 20 also recite the step of sputtering the impurity solid utilizing ions in the plasma ***so as to mix the impurity into the plasma***. Thereafter, a

voltage is applied to the semiconductor substrate to create a difference of potential between the plasma and the substrate, ***such that the impurity mixed in the plasma is directly driven into the surface of the substrate***.

In contrast to the present invention, the formation of ***impurity layer 38 of Booske occurs prior to the generation of plasma***. More specifically, as set forth on col. 10, lines 18-27, sputter deposition of the target 46 is conducted in order to form the impurity layer 38 on the surface of the substrate. Importantly, however, during this sputtering process, there is no plasma in the chamber. After the impurity layer 38 is formed, plasma source ion implantation is utilized to achieve implantation of the dopant atoms contained in the impurity layer 38 into the substrate. As such, the process of Booske does not result in the impurity being mixed into the plasma, and therefore it also does not drive an impurity contained in the plasma into the surface of the substrate. ***Thus, Booske also fails to disclose or suggest (1) mixing the impurity into the plasma, or (2) implanting the impurity mixed into the plasma directly into the surface of the substrate, both or which are recited by the rejected claims.***

Based on the foregoing operation of Booske, it is believed to be clear that Booske's process is significantly different from the claimed invention.

Accordingly, as each and every claim limitation must be disclosed or suggested by the cited prior art references in order to substantiate a rejection under 35 U.S.C. § 103 (*see*, M.P.E.P. § 2143.03), and the foregoing makes clear that Booske and Wolf fail to do so, it is submitted that claims 1 and 20 are patentable over both Booske and Wolf, taken alone or in combination with one another.

III. The Rejection Of Claims 7, 9, 11-13, 26, 28 And 30-32 Under 35 U.S.C. § 103

Claims 7, 9, 11-13, 26, 28 and 30-32 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era, and further in view of JP 05024976 to Nakagawa. Applicants respectfully traverse this rejection for the following reasons.

First, claims 7 and 26, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, as the newly cited reference, Nakagawa, is not relied upon as curing the deficiencies of Booske noted above, it is respectfully submitted that claims 7 and 26 are patentable over the cited combination of prior art for the same reasons as set forth in Section II.

Further, as recited by claims 7 and 26 of the present invention a first voltage is applied to the impurity solid so as to allow the impurity solid to serve as a cathode for the plasma. Thus, the electrode applying the first voltage is a cathode. Further, a second voltage is applied to the semiconductor substrate so as to allow the substrate to serve as an anode for the plasma. Thus, the electrode applying the second voltage is an anode. In contrast, according to Nakagawa, a sample 105 is connected with an anode 103 and a target 109 is connected with a cathode 104. Thus, the relationship of the anode and cathode relative to the target and substrate are reversed in Nakagawa. Accordingly, Nakagawa fails to disclose this limitation recited by claims 7 and 26.

IV. The Rejection Of Claims 14, 16, 18, 19, 33, 35, 37 And 38 Under 35 U.S.C. § 103

Claims 14, 16, 18, 19, 33, 35, 37 and 38 were rejected under 35 U.S.C. § 103 as

being obvious over USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era, and further in view of JP 05024976 to Nakagawa and USP No. 4,596,645 to Stirn. Applicants respectfully traverse this rejection for the following reasons.

Claims 14 and 37, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, as the newly cited reference, Stirn, is not relied upon as curing the deficiencies of Booske noted above, it is respectfully submitted that claims 14 and 37 are patentable over the cited combination of prior art for the same reasons as set forth in Section II.

Accordingly, it is respectfully requested that the rejection be withdrawn.

V. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all pending independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

VI. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 3/17/03

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